

## BEST AVAILABLE COPY

Application No.: 10/065,524

Docket No.: JCLA8269

### AMENDMENTS

#### In The Claims:

Please amend the claims as indicated hereafter.

**Claim 1. (previously presented)** A method of hot switching a data transfer rate on a bus, to dynamically switch the data transfer rate on the bus between a first control chip and a second control chip, comprising the steps of:

the first control chip and the second control chip receiving a transfer rate switching command;

when either there is no data transaction processed or the data transaction process is finished, the first control chip issuing a bus release connect command;

the first control chip and the second control chip entering into the bus release connect state according to the bus release connect command;

either the first control chip or the second control chip issuing a bus re-connect command; and

the first control chip and the second control chip re-connecting to the rated-changed bus according to the transfer rate switching command.

**Claim 2. (original)** The method of hot switching data transfer rate on the bus of claim 1, wherein the first control chip is a north-bridge chip, and the second control chip is a south-bridge chip.

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**Claim 3. (original)** The method of hot switching data transfer rate on the bus of claim 2, wherein the data transfer rate is switched between four times the north-bridge chip clock frequency and eight times the north-bridge chip clock frequency.

**Claim 4. (original)** The method of hot switching data transfer rate on the bus of claim 1, wherein the first control chip and the second control chip both have a transfer rate register for temporarily storing the transfer rate switching command.

**Claim 5. (currently amended)** A method of hot switching a data transfer rate on a bus, comprising the steps of:

receiving a transfer rate switching signal before data transfer on the bus between a first control chip and a second control chip is interrupted; and

after states of ~~when~~ the first control chip and the second control chip are changed from ~~[[in]]~~ a bus release state ~~and then~~ into a re-connecting state, providing another data transfer rate to the bus according to the transfer rate switching signal.

**Claim 6. (original)** The method of hot switching data transfer rate on the bus of claim 5, wherein the first control chip is a north-bridge chip, and the second control chip is a south-bridge chip.

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**Claim 7. (original)** The method of hot switching data transfer rate on the bus of claim 6, wherein the data transfer rates at least comprise four times the north-bridge chip clock frequency and eight times the north-bridge chip clock frequency.

**Claim 8. (original)** The method of hot switching data transfer rate on the bus of claim 5, wherein the first control chip and the second control chip both have a transfer rate register for temporarily storing the transfer rate switching command.

**Claim 9. (previously presented)** A method of hot switching a data transfer rate on a bus, to dynamically switch a plurality of data transfer rates on the bus between a first control chip and a second control chip, comprising the steps of:

the first control chip and the second control chip receiving a data transfer rate switching command, and temporarily storing the data transfer rate switching command into transfer rate registers of the first control chip and the second control chip;

when either there is no data transaction processed or the data transaction process is finished, issuing a bus release connect command to have the first control chip and the second control chip enter into a bus release connect state; and

when either the first control chip or the second control chip issues a bus re-connect command, the first control chip and the second control chip switching to one of the data transfer rates on the bus according to contents of the transfer rate registers.

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**Claim 10. (original)** The method of hot switching data transfer rate on the bus of claim 9, wherein the first control chip is a north-bridge chip, and the second control chip is a south-bridge chip.

**Claim 11. (original)** The method of hot switching data transfer rate on the bus of claim 10, wherein the data transfer rates at least comprise four times the north-bridge chip clock frequency and eight times the north-bridge chip clock frequency.